Prior Art: Memory Bus

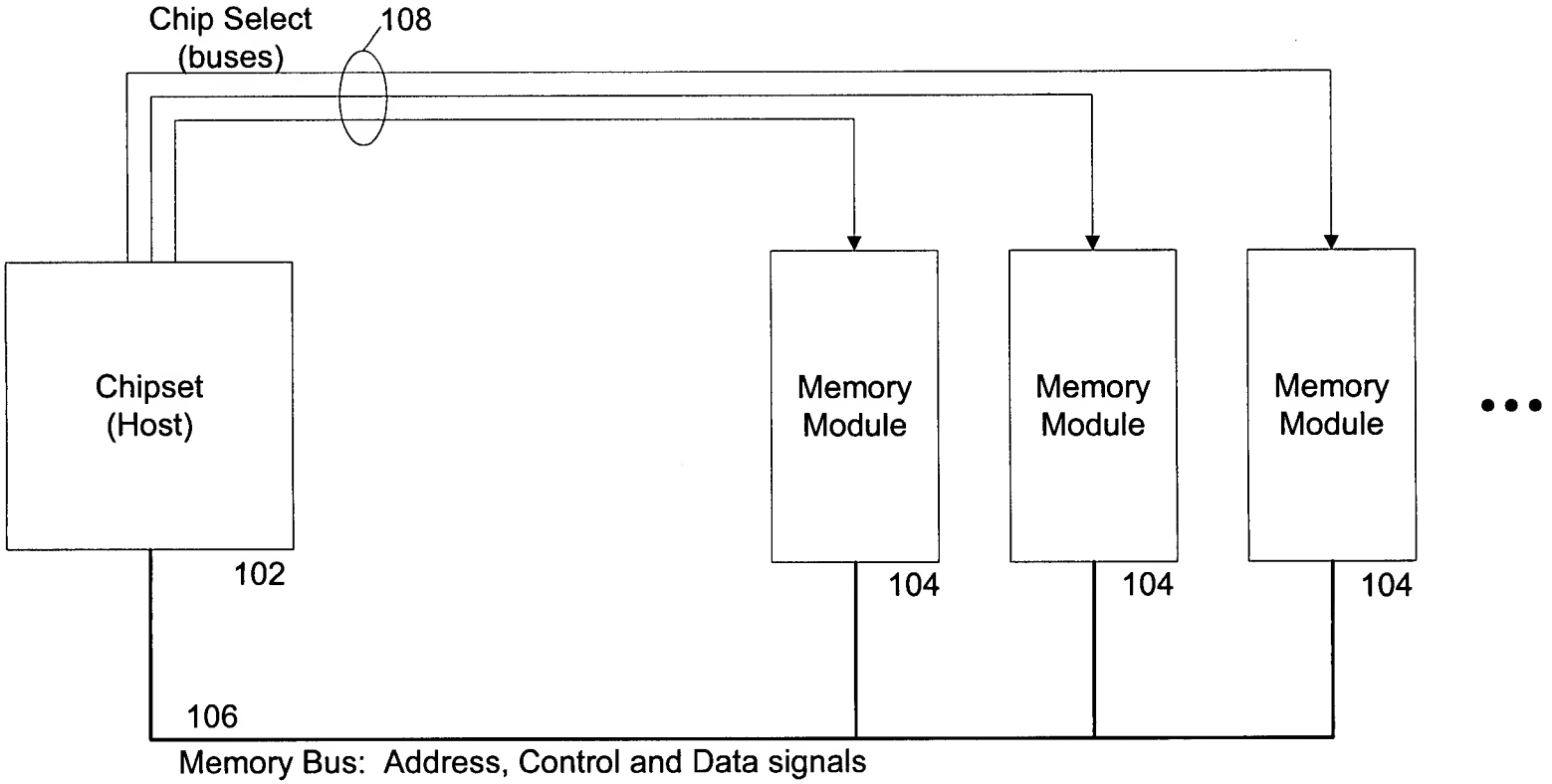

Figure 1

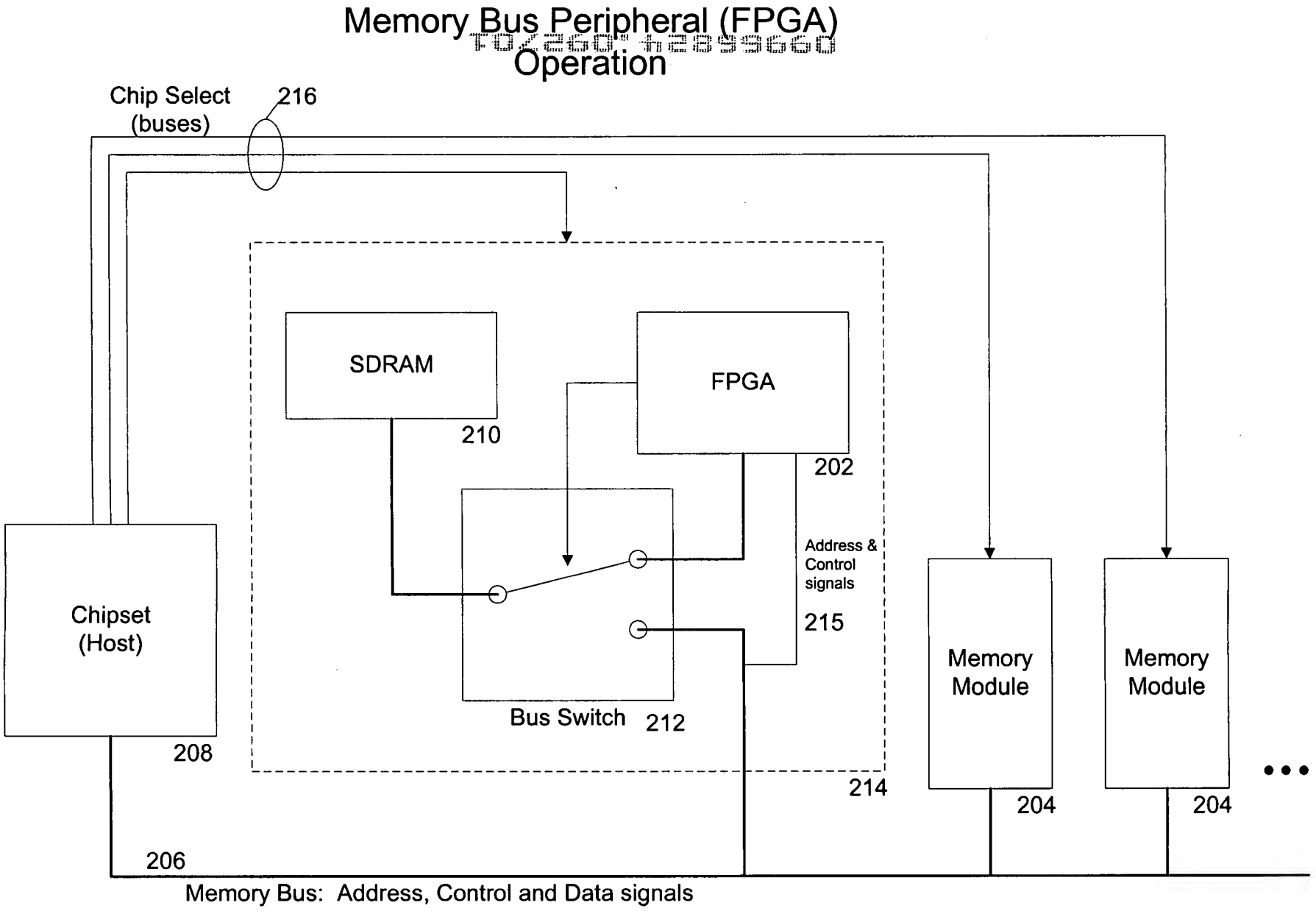
Memory Bus Peripheral (FPGA)
Operation
Chip Select
(buses)
216
SDRAM
210
FPGA
202
Address &
Control
signals
215
Chipset
(Host)
208
Bus Switch
212
214
Memory
Module
204
Memory
Module
204
206
Memory Bus: Address, Control and Data signals

Figure 2

Operational Flowchart

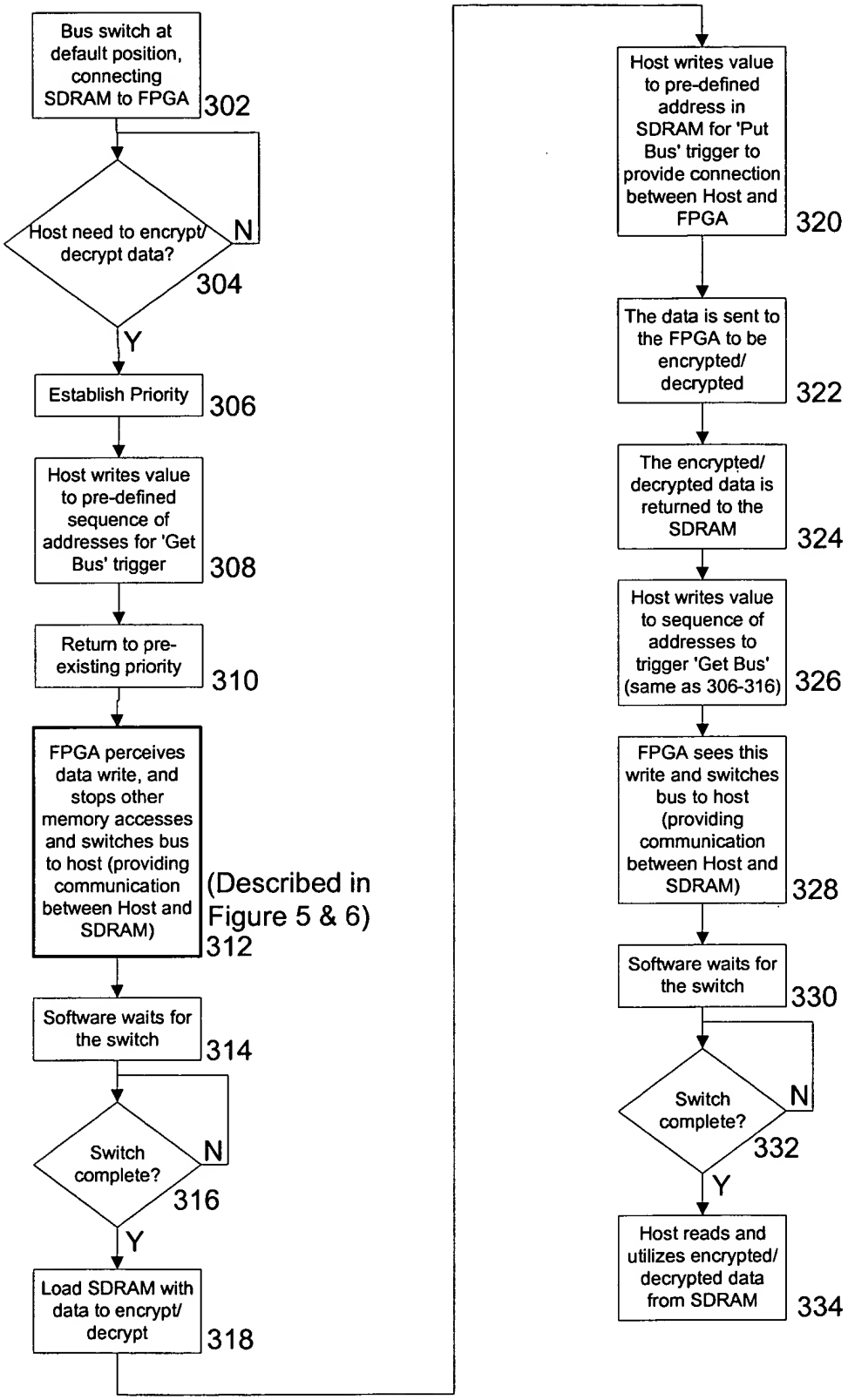

Figure 3

Example Memory Module Trigger Address Locations

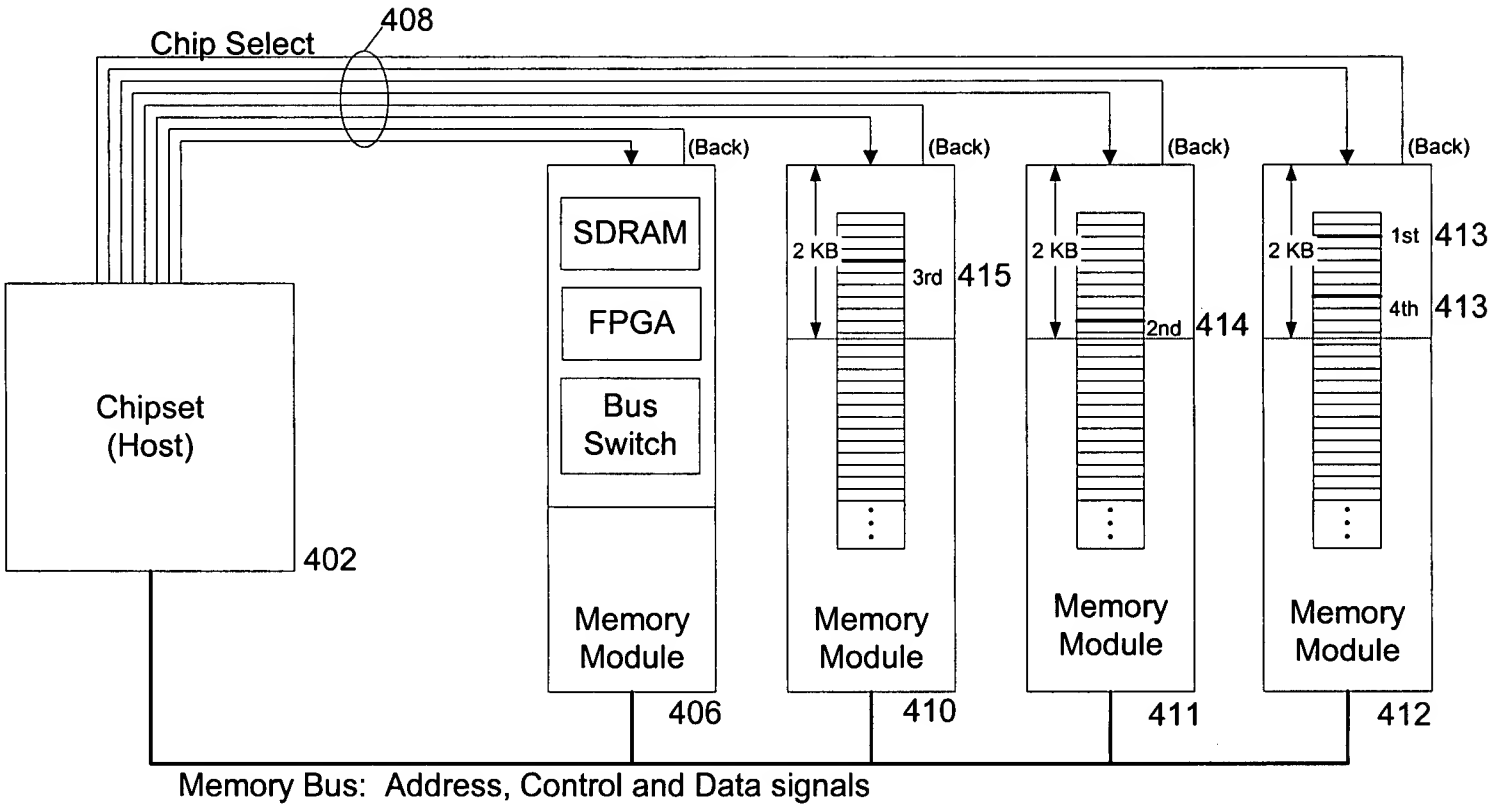

Figure 4

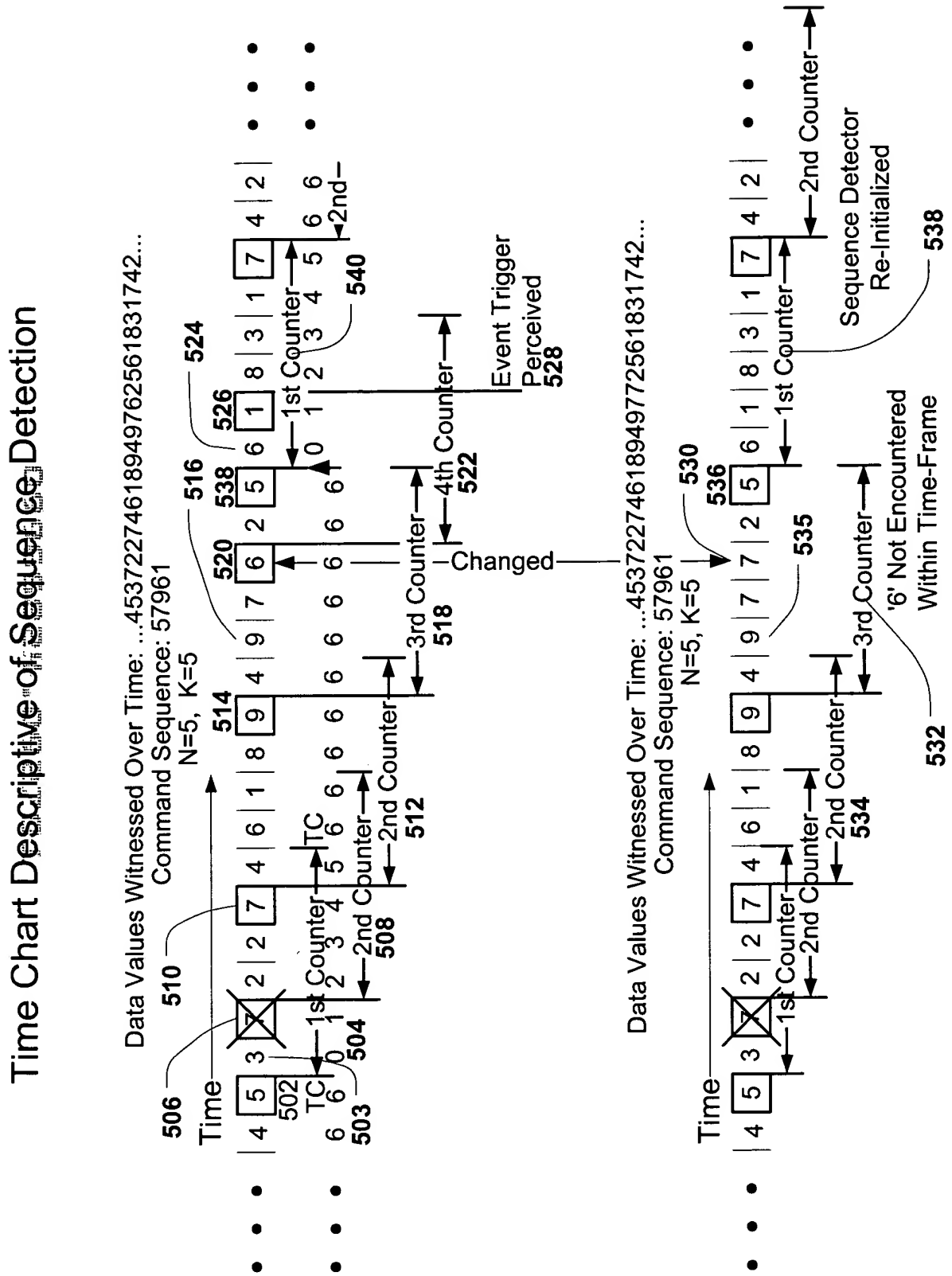
Time Chart Descriptive of Sequence Detection
Data Values Witnessed Over Time: ...4537227461894976256183174 2...
Command Sequence: 57961
N=5, K=5
Time
506
510
502
503
504
TC
1st Counter
2nd Counter
508
512
514
516
518
3rd Counter
520
522
4th Counter
524
526
538
540
2nd
Event Trigger
Perceived
528
Changed
Data Values Witnessed Over Time: ...4537227461894976256183174 2...
Command Sequence: 57961
N=5, K=5
530
536
535
534
532
'6' Not Encountered
Within Time-Frame
Sequence Detector
Re-Initialized
538

Figure 5

General Schematic of Data Value Sequence Detector "1010"

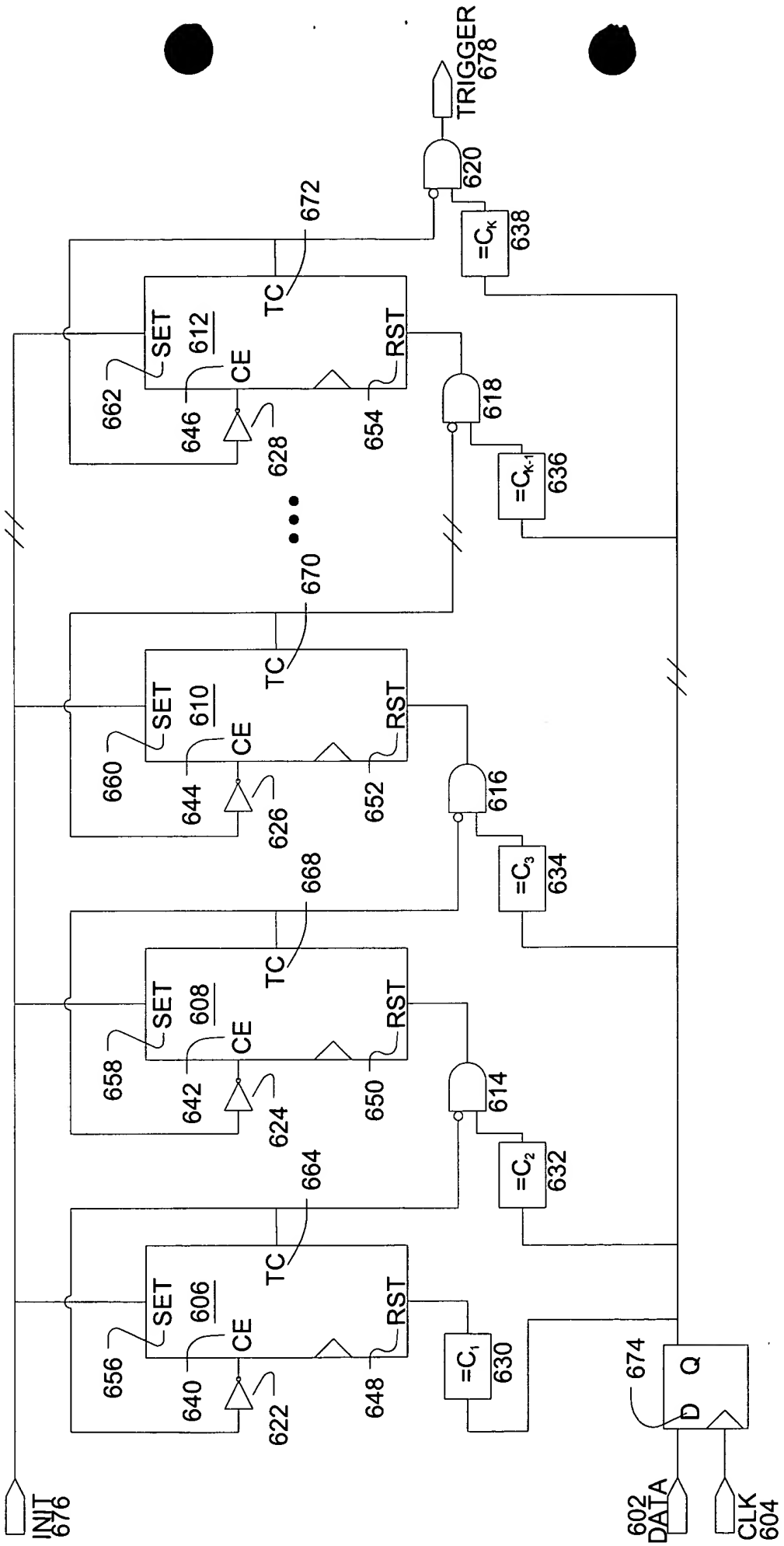

Figure 6